



1/5
FIG. 1A

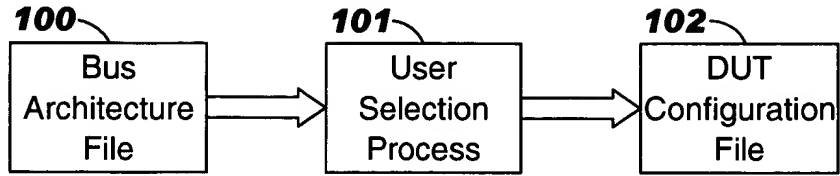


FIG. 1B

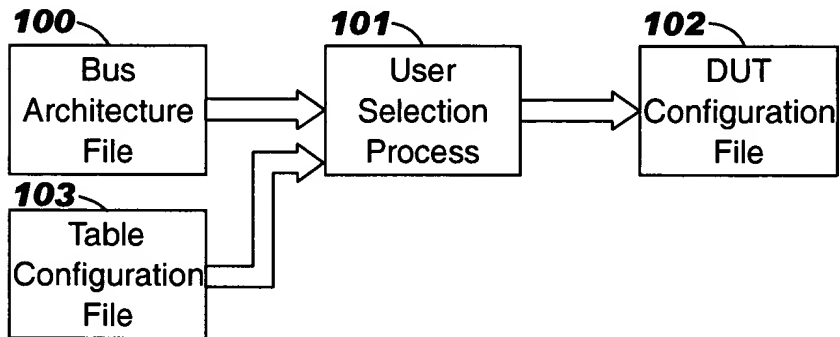


FIG. 1C

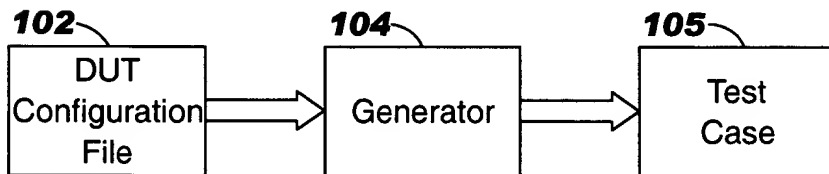


FIG. 1D

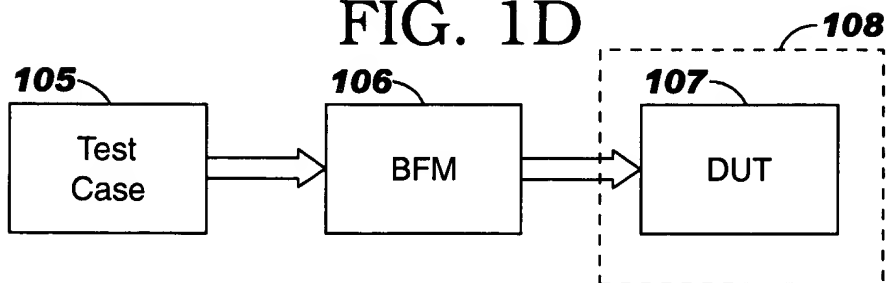


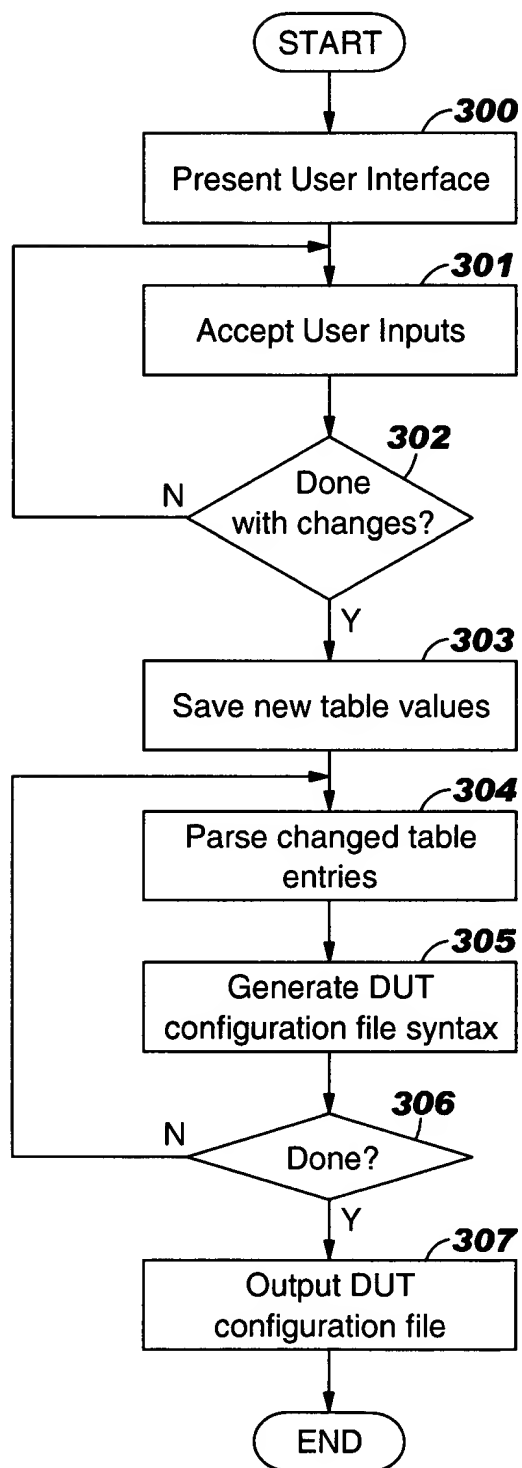
FIG. 2

Address Range: 0x20000000 to 0x4FFFFFFF		uniform
<input type="checkbox"/> Single Transfers <input type="checkbox"/> Burst Transfers		
Burst Transfer Widths: <input type="checkbox"/> byte <input type="checkbox"/> half-word <input type="checkbox"/> word <input type="checkbox"/> double-word <input type="checkbox"/> quad-word <input type="checkbox"/>		
<input type="checkbox"/> Fixed-Length Burst Transfers		
Fixed Burst Transfer Lengths: <input type="checkbox"/> 1 <input type="checkbox"/> 2 <input type="checkbox"/> 3 <input type="checkbox"/> 4 <input type="checkbox"/> 5 <input type="checkbox"/> 6 <input type="checkbox"/> 7 <input type="checkbox"/> 8 <input type="checkbox"/> 9 <input type="checkbox"/> 10 <input type="checkbox"/> 11 <input type="checkbox"/>		
<input type="checkbox"/> Variable-Length Burst Transfers		
Variable Burst Deassert Delay: 1 to 16		
<input type="checkbox"/> Line Transfers		
Line Transfer Lengths: <input type="checkbox"/> 4-word <input type="checkbox"/> 8-word <input type="checkbox"/> 16-word		
Line Read Word Mode: <input type="checkbox"/> sequential <input type="checkbox"/> target word first		
Master Data Bus Width: <input type="checkbox"/> 32 <input type="checkbox"/> 64 <input type="checkbox"/> 128		
Request Delay Range: 0 to 7		
Locked Transfers: <input type="checkbox"/> locked <input type="checkbox"/> unlocked <input type="checkbox"/> both		
Lock Deassert Delay: 1 to 6		
Transfer Types: <input type="checkbox"/> memory <input type="checkbox"/> plb slave buffered		
Compressed Transfers: <input type="checkbox"/> compressed <input type="checkbox"/> non-compressed <input type="checkbox"/> both		
Guarded Transfers: <input type="checkbox"/> guarded <input type="checkbox"/> non-guarded <input type="checkbox"/> both		
Ordered Transfers: <input type="checkbox"/> ordered <input type="checkbox"/> non-ordered <input type="checkbox"/> both		
Lock Error Registers: <input type="checkbox"/> lockerr <input type="checkbox"/> non-lockerr <input type="checkbox"/> both		
Abort Transfers: <input type="checkbox"/> abort <input type="checkbox"/> non-abort <input type="checkbox"/> both		
Abort_Assert Delay: 1 to 16		
Master Priority: <input type="checkbox"/> 00 <input type="checkbox"/> 01 <input type="checkbox"/> 10 <input type="checkbox"/> 11		





3/5
FIG. 3





4/5
FIG. 4

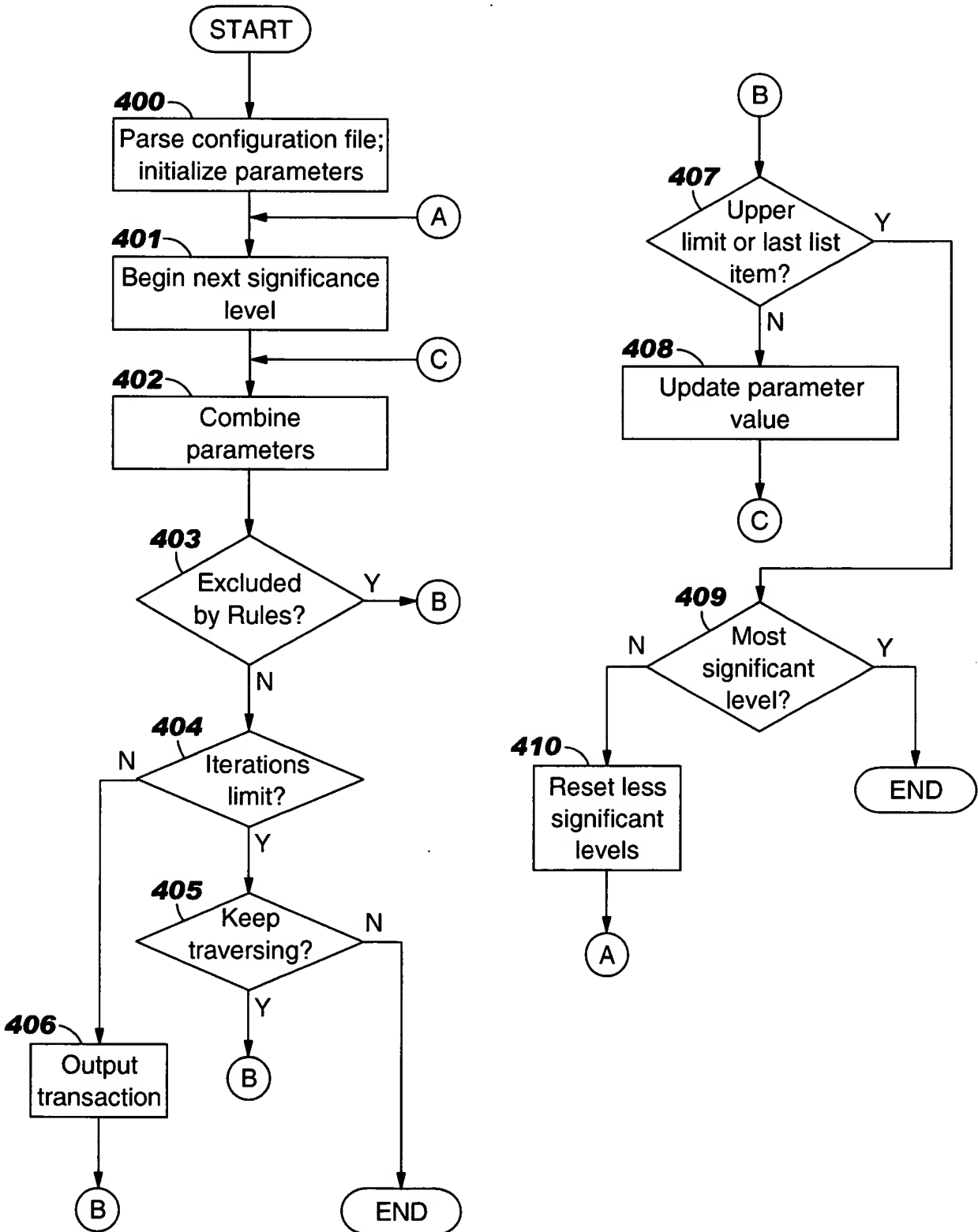




FIG. 5

